Implementation of 555 Timer on Cypress Programmable System on Chip

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ABSTRACT:
Cypress PSoC (Programmable System on Chip) is a device that consists of programmable analog blocks, programmable digital blocks and an MCU. Any single circuit worthy of construction can be built with 555 timer(Pulse Extender Circuit).The 555 timer IC can be used in a variety of timer, pulse generation, oscillator applications, to provide time delays, and as a flip-flop element. It provides circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for both mono-stable and astable applications.555timer is designed in a PSoC device and is being used to generate square pulse and delays for different electronic devices. 555 timer designed using both the digital and analog blocks of cypress PSoC. Dynamic reconfiguration is an extremely powerful feature of the PSoC device. It enables a designer to program multiple configurations within their design and then dynamically change those configurations while the device is running. The paper will demonstrate the methodology of designing the square wave generator and its configuration on the PSoC creator, a module of cypress PSoC. It follows that if the PSoC can simulate a 555 timer, then PSoC can be used to design any circuit of significance.

Keywords - Cypress PSoC development kit(001), miniprog3, PSoC1, PSoC designer.

I. INTRODUCTION

Dynamic reconfiguration is an extremely powerful feature of the PSoC device. It enables a designer to program multiple configurations within their design and then dynamically change those configurations while the device is running [1].
The paper will demonstrate the methodology of designing the square wave generator and its configuration on the PSoC designer, a module of cypress PSoC .

II. THEORY

The 555 timer IC is used in a variety of timer, pulse generation, and oscillator applications. The 555 timer consists of two voltage comparators, a flip-flop, a discharge transistor, an output stage and a resistor divider network. Resistor R_1 is connected between V_{CC} and the discharge, another resistor R_2 is connected between the discharge pin, the trigger and threshold pins that share a common node. Hence the capacitor is charged through R_1 and R_2, and discharged only through R_2, since discharge pin has low impedance to ground during output low intervals of the cycle, therefore discharging the capacitor [2].
The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally to 2/3 of supply voltage and the trigger comparator is referenced to 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop [3]. A block diagram is shown is Fig.

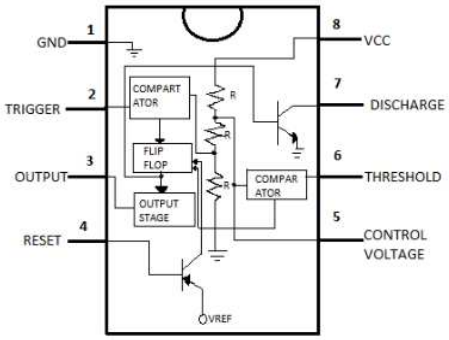

figure1: 555 Timer Block Diagram

III. METHEDOLOGY

All the module of cypress PSoC have Flash memory to store their configuration. The chip can be easily reprogrammed with the correct configuration. We configure the pin configuration on the PSoC designer by assigning the ports with different pin as per given in the circuit below in Fig2.

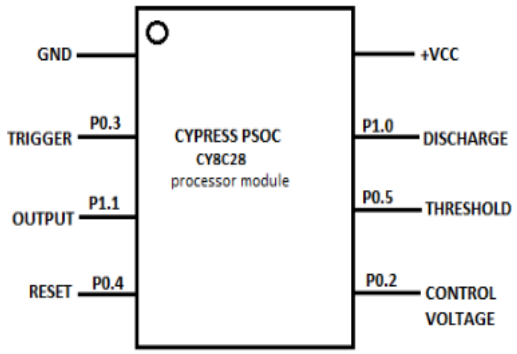

figure2. 555 Timer Pinout

Reset is actually configured as a pull-up output. When logic high is written to the data register for this pin, it appears as a resister pulling this pin to V_{cc}. ResetCmp is a comparator that converters this analog signal back to a digital level accessible to the digital blocks equation (1) defines the logical equation to implement [3].

Output=((output*!Threshold)+!Trigger)*Reset**(1)**

Discharge= output.

The digital blocks which is configured as buffers, along with global logic connections are used to implement Equation (1).
The digital blocks are configured as per the configuration done in PSoC designer which is shown below in Fig.

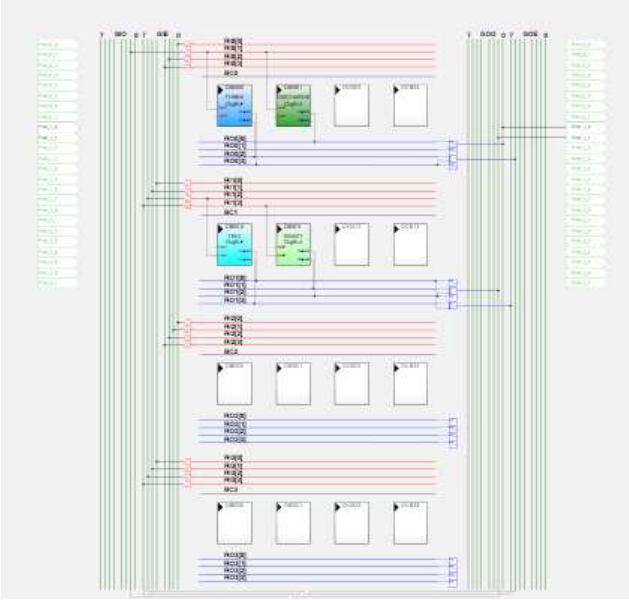

figure3. digital block configuration of designer

Analog blocks are configured in similar manner which is show below in Fig.

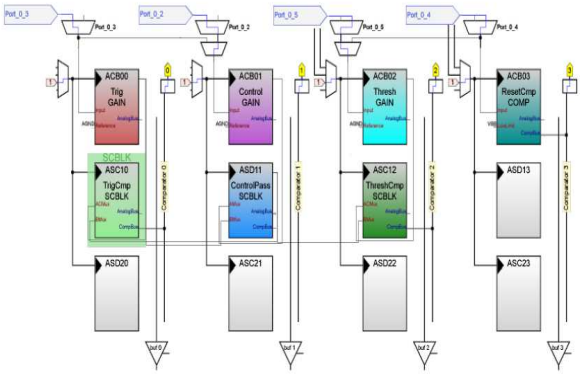

figure4. Analog block configuration on PSoC designer

We build all project and simulate the project. After that we program the development kit (DVK) board with miniprog3 and then we configure hardware to check its output.

IV. RESULT

When the output is high, the discharge path is open and capacitor charges through R_1 and R_2. This continues until the capacitor voltage reaches the threshold value causing the output to turn off. When the output is low, the discharge path closes and the capacitor discharges through R_2 to ground. When the capacitor voltage drops to the trigger value, the output goes high and the cycle starts again

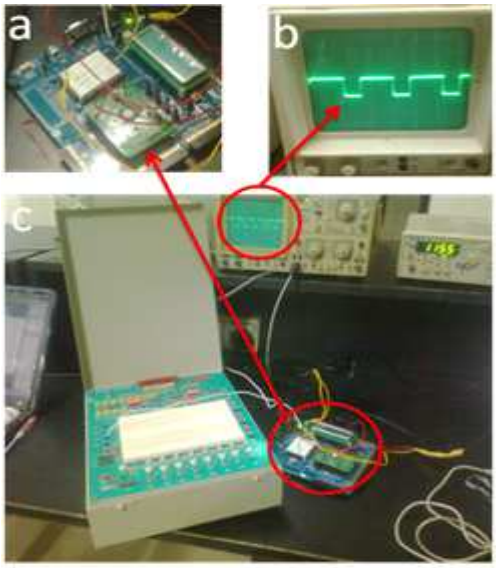

figure5. (a) Cypress Developer Board CY8CKIT-001, (b) ASIC based result for 555 implemented on PSoC, (c) A complete snap of experimental setup.

V. CONCLUSION

The 555 timer that has been successfully simulated on PSoC. This IC which is design on cypress PSoC can be used to build a lot of different circuits. It can be used in variety of timer, pulse generation, and oscillator applications.

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